REMARKS

This Preliminary Amendment is filed with a Request for Continued Examination filed on even date herewith in response to the Final Office Action mailed on October 27, 2004. All objections and rejections are respectfully traversed.

Claims 1-66 are cancelled.

Claims 67 – 117 were added to better claim the invention.

Applicant wishes to express gratitude for Examiner's phone interview on April 13, 2005.

At paragraphs 8-13 of the Final Office Action, previous claims 1-21, 28-36, and 38-66 were rejected under 35 U.S.C. §103 as being unpatentable over Nakada, U.S. Patent No. 5,638,526 issued June 10, 1997, in view of Asato, U.S. Patent No. 6,145,074 issued November 7, 2000. Claims 1-66 have been canceled, and all new claims 67-117 are believed to be in condition for allowance.

In particular, the present invention, as set forth in representative new claim 67, comprises in part:

67. A processor, comprising:

. . .; and

a mulitplexer (MUX) having i) a first input coupled to the first input of the first ALU, ii) a second input coupled to the first input register of the second ALU, and iii) an output directly providing a first input to the second ALU, the MUX permitting both the first and second ALU to share the source operand stored in the first input register of the first ALU.

Nakada discloses an apparatus for operand data bypassing having an operand storage register connected between an input selector and the ALU. Nakada controls the input selector by a comparator circuit (COMP), which detects a coincidence between the contents of a preceding register number in an instruction and the register number of the next instruction. When this coincidence is detected, the COMP circuit selects either a cache register (which is a copy of the operand storage register) or the result from the ALU as the input to the selector.

Asato discloses a system for selecting a standard register or previous instruction RESULT bypass as a source operand path based on a bypass specifier field in a succeeding instruction. Asato uses this bypass field as an indication of whether a register in an instruction is the RESULT of a previous instruction. An instruction in Asato will specify if the registers of an instruction are the RESULT of a previous instruction, either by the use of a bypass field, or by addressing a RESULT bypass input line from the pipeline.

Applicant respectfully urges that neither Nakada nor Asato show Applicants claims novel "***mulitplexer (MUX) having i) a first input coupled to the first input of the first ALU, ii) a second input coupled to the first input register of the second ALU, and iii) an output directly providing a first input to the second ALU.***"

Applicant claims a system and method for directly addressing various pipeline stage registers of a plurality of execution units in a processing engine. By directly addressing the registers, the plurality of execution units can utilize source operand bypassing by, for example, sharing source operands and/or results, without having to read a register file. Applicant's claimed use of ***directly providing*** the first input to the second ALU from the first input to the first ALU, addresses of desired data need not be repeated, whether they are internal register addresses or external memory addresses (which can be

very long). Neither Nakada nor Asato discuss a multiplexer's ***output directly providing a first input to the second ALU*** as in Applicant's claims.

Applicant respectfully urges that the Nakada patent and the Asato patent, either taken singly or in any combination are legally insufficient to render the presently claimed invention obvious under 35 U.S.C. §103 because of the absence in each of the cited patents of Applicant's claimed novel "***mulitplexer (MUX) having i) a first input coupled to the first input of the first ALU, ii) a second input coupled to the first input register of the second ALU, and iii) an output directly providing a first input to the second ALU.***"

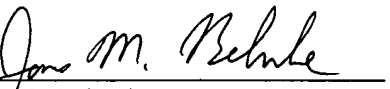
All independent claims are believed to be in condition for allowance.

All dependent claims are believed to be dependent from allowable independent claims, and therefore in condition for allowance.

Favorable action is respectfully solicited.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,



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